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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,624	01/24/2006	Jun Suda	HIRA.0217	2518

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EXAMINER	
AHMED, SELIM U	
ART UNIT	PAPER NUMBER
2826	

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12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,624	SUDA ET AL.	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-33* is/are pending in the application.

4a) Of the above claim(s) *22-24* is/are withdrawn from consideration.

5)☒ Claim(s) *18-21,27-31 and 33* is/are allowed.

6)☒ Claim(s) *11-17,25, 26, 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, including claims 11-21 and 25-33 in the reply filed on 09/24/2008 is acknowledged.

2. The Preliminary Amendments filed on 01/24/2006 and 09/24/2008 has been entered.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 01/24/2006.

Information Disclosure Statement

4. The Information Disclosure Statements filed on 12/11/ 2006 and 07/19/2007 has been considered.

Oath/Declaration

5. The oath or declaration filed on 01/24/2006 is acceptable.

Drawings

6. The drawings filed on 01/24/2006 are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11-17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 5,900,648; Harris hereinafter) in view of Arai et al (JP 2000-150792; Arai hereinafter. Please note that applicant provided this reference on 01/24/2006).

With regard to claim 11, Harris discloses a field effect transistor e.g. Fig. 1, comprising: a SiC surface structure 1; a source 2 and a drain 3 formed in said SiC surface structure; an interface control layer 4 formed adjacent to said SiC surface structure and comprising a Group-III nitride layer (e.g. abstract), said interface control layer having a film thickness in the range of one molecule-layer to a critical film thickness such that no misfit dislocation occurs with said SiC surface structure (Abstract; since lattice is substantially matched it is reasonable to assume that film thickness is in the range of one molecule layer to a critical film thickness); and a gate electrode 5 formed on said insulating structure.

As discussed above, Harris discloses all of the limitations of claim 1 with the exception of an insulating structure comprising an insulating layer

formed on said interface control layer from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer. However, e.g. Fig.1-2, claims 1-4, para[0005, 0010, 0029] of Arai discloses an insulating structure comprising an insulating layer (i.e. Al2O3) formed on said interface control layer from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer. It would have been obvious to one having ordinary skill in the art at the time of the invention to include an insulating structure comprising an insulating layer formed on said interface control layer from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer for predictable result. For example, para[0005, 0010, 0029] of Arai discloses that including such an insulating structure comprising an insulating layer would solve the problem of high degree of interface states and thus increasing the breakdown voltage i.e. 10MV/cm.

With regard to claim 12, e.g. claim 1 of Harris discloses the field effect transistor wherein said Group-III nitride layer comprises AlN. Furthermore, Harris discloses the claimed invention except for the thickness of AlN being less than 6 nm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form 6 nm or less AlN through routine

experimentation. Also, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

With regard to claim 13, e.g. claim 1 of Harris discloses the field effect transistor wherein said interface control layer comprises a Group-III element including at least one of B, Al, Ga, or In, and N.

With regard to claim 14, e.g. col.3, lines 29-47 of Harris discloses the field effect transistor according to claim 11, wherein said interface control layer comprises a BAlN layer (e.g. Group III-B) whose in-plane lattice constant has a mismatch of 0.5% or smaller with respect to the in-plane lattice constant of SiC (inherent).

With regard to claim 15, e.g. para[0010] of Arai discloses the field effect transistor, wherein said insulating layer includes at least one layer selected from the group consisting of a SiO2 layer, a SixNy layer, and an A1203 layer. It would have been obvious to one having ordinary skill in the art at the time of the invention to include such an insulating structure that would solve the problem of high degree of interface states and thus increasing the breakdown voltage i.e. 10MV/cm.

Applicant's claim 16 do not distinguish over the Harris in view of Arai reference regardless of the process used to form the Al2O3 because only the final product is relevant, not the process of making such as "formed by oxidizing a deposition layer of at least one material selected from the group consisting of AlN, Al, AlxNy, AlAs, and AlNxASl_x". Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claim 17, e.g. claim 3 of Arai discloses the field effect transistor, wherein said insulating layer has a multilayered film comprised of a plurality of insulating films.

With regard to claim 32, e.g. Fig.1, element 8 of Harris discloses an electrode to said drain of claim 11 is formed to arbitrary position including front or back side of said SiC surface layer.

With regard to claim 25, Harris discloses a field effect transistor e.g. Fig.1 comprising: a SiC surface structure 1; a source 2 and a drain 3 formed in said SiC surface structure; a single-layer 4 or multilayer insulating structure comprising an interface control layer 4 and an insulating layer, wherein said interface control layer is formed adjacent to said SiC surface structure e.g. Fig. 1, contains Al and N (Abstract), and has a thickness of one molecule layer or greater (inherent), and a gate electrode formed on said insulating structure 5.

As discussed above, Harris discloses all of the limitation of claim 25 with the exception the single or multilayer insulating structure comprising an insulation layer wherein said insulating layer is formed on said interface control layer from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer, wherein said insulating layer is either an A1203 layer or an A1203 layer that contains a small amount of at least one of N or As. However, e.g. Fig.1-2, claims 1-4, para[0005, 0010, 0029] of Arai discloses the single or multilayer insulating structure comprising an insulation layer wherein said insulating layer is formed on said interface control layer from a material that is different from said interface

control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer, wherein said insulating layer is either an A1203 layer or an A1203 layer that contains a small amount of at least one of N or As. It would have been obvious to one having ordinary skill in the art at the time of the invention to include the single or multilayer insulating structure comprising an insulation layer wherein said insulating layer is formed on said interface control layer from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer, wherein said insulating layer is either an A1203 layer or an A1203 layer that contains a small amount of at least one of N or As for predictable result. For example, para[0005, 0010, 0029] of Arai discloses that including such an insulating structure comprising an insulating layer would solve the problem of high degree of interface states and thus increasing the breakdown voltage i.e. 10MV/cm.

Furthermore, Applicant's claim 25 do not distinguish over the Harris in view of Arai reference regardless of the process used to form the Al2O3 because only the final product is relevant, not the process of making such as "formed by oxidizing a deposition layer of at least one material selected from the group consisting of AIN, A1, AlxNy, AlAs, and A1NxAs1_x,". Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685;

In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claim 26, e.g. claim3, para[0010] of Arai discloses the field effect transistor according to claim 25, wherein said insulating layer includes a double-layered film structure on said interface control layer, said double-layered film structure comprising an A1203 layer and a SiO2 layer in order.

Allowable Subject Matter

8. Claims 18-21, 27-33 allowed.

The following is a statement of reasons for the indication of allowable subject matter:

With regard to claim 18, the prior art of record fail to teach or suggest a non-volatile memory element especially with a floating-gate structure formed on SiC surface structure, wherein said floating-gate structure includes an interface

control layer, a first insulator barrier layer, a floating-gate layer formed of a metal or a semiconductor quantum well, a second insulator barrier layer, and a gate electrode layer, wherein said interface control layer is a Group-III nitride layer formed in contact with said SiC surface structure as in the combination of claim 18.

With regard to claim 27, the prior art of record fail to teach or suggest a nonvolatile memory element especially with a floating-gate structure formed on said SiC surface structure including a first insulator barrier layer, a well layer, a second insulator barrier layer, and a gate electrode layer, wherein said first insulator barrier layer is formed in contact with said SiC surface structure and comprises a Group-III nitride epitaxial layer, said well layer is formed of a Group-III nitride epitaxial layer and functions as a floating gate, and said second insulator barrier layer is formed of a Group-III nitride epitaxial layer as in the combination of claim 27.

The dependent claims are allowable for at least the same reason as base claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

/Evan Pert/
Primary Examiner, Art Unit 2826